THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 401 – Analog CMOS Integrated Circuit Design
Final Exam
Due: Saturday, December 18th, 2021 at 11:59 pm (Pacific Time)

This is an open book take-home exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Please do not consult and/or discuss the questions and/or your solutions with anyone before the due date shown above. Your solutions/answers should be based on your individual effort! Please also note that each question has its own transistor parameters.

Good luck!

This exam has 6 questions and including the cover page consists of 18 pages. The 6th question is a bonus question, and it offers up to 10 bonus marks, so we could get up to 110% out of this exam!

Shanks Cole
Surname First name

Student Number 54950860
Student Number

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
5	20	
6	10	
TOTAL	110	

READ THIS

Candidates who commit to any of the following, or similar, dishonest practices shall be liable to disciplinary action:

Speaking or communicating with other candidates or non-candidates regarding the exam questions.

Purposely exposing their solution to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. In the following circuit assume:
$\lambda_{(NMOS)}=0$ V^{-1}, $\lambda_{(PMOS)}=0.05$ V^{-1}, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=0.1$ mA/V^2, $\mu_p C_{ox}=0.05$ mA/V^2, and $\gamma_{(NMOS)}=\gamma_{(NMOS)}=0$.

Further, assume that the DC current of M_1 and M_2 is 1 mA each and that of M_3 and M_4 is 0.5 mA each. Assume all transistors are in operating in saturation region and the aspect ratio of transistors is as follows:
$(W/L)_1 = 125$, $(W/L)_2 = 250$, $(W/L)_3 = 40$, and $(W/L)_4 = 80$.

a) Find transconductance (g_m) of all the transistors and the drain-source resistance (r_o) of the PMOS transistors, that is, r_{o2} and r_{o4}. **[10 marks]**

b) Find the voltage gains V_{out1}/V_{in} and V_{out2}/V_{in}. **[10 marks]**

NMOS: $V_D > V_G - V_{th}$

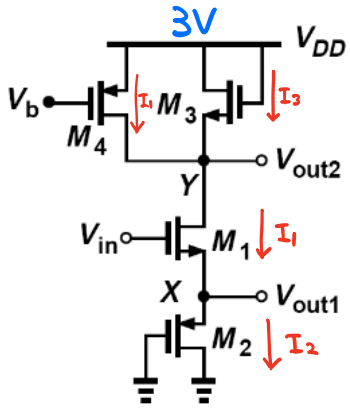
$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2$

PMOS: $V_D < V_G - V_{th}$

$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right) (V_{SG} - V_{th})^2$

$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$

$r_o = \frac{1}{\lambda I_D}$



M_1:

$g_{m_1} = \sqrt{2 \cdot 0.1\times10^{-3} \cdot 125 \cdot 1\times10^{-3}}$

$g_{m_1} = 5m\,A/V$

M_3:

$g_{m_3} = \sqrt{2 \cdot 0.1\times10^{-3} \cdot 40 \cdot 0.5\times10^{-3}}$

$g_{m_3} = 2m\,A/V$

M_2:

$r_{o_2} = \frac{1}{0.05 \cdot 1\times10^{-3}}$

$r_{o_2} = 20k\Omega$

$g_{m_2} = \sqrt{2 \cdot 0.05\times10^{-3} \cdot 250 \cdot 1\times10^{-3}}$

$g_{m_2} = 5m\,A/V$

M_4:

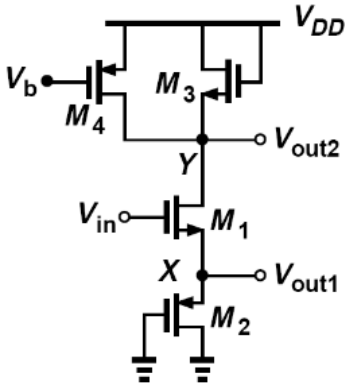
$r_{o_4} = \frac{1}{0.05 \cdot 0.5\times10^{-3}}$

$r_{o_4} = 40k\Omega$

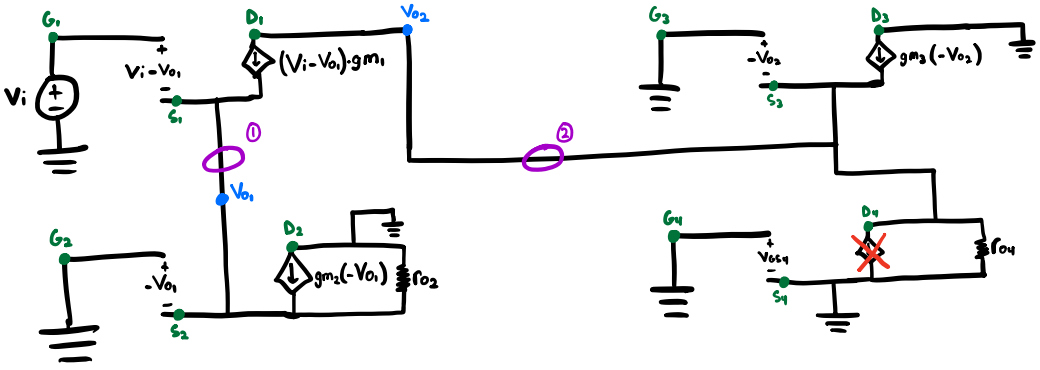
$g_{m_4} = \sqrt{2 \cdot 0.05\times10^{-3} \cdot 80 \cdot 0.5\times10^{-3}}$

$g_{m_4} = 2m\,A/V$

For your convenience the circuit and its parameters are duplicated below:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0.05\ V^{-1}$, $V_{DD}=3.0\ V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=0.1\ mA/V^2$, $\mu_p C_{ox}=0.05\ mA/V^2$, and $\gamma_{(NMOS)}=\gamma_{(NMOS)}=0$.
$(W/L)_1 = 125$, $(W/L)_2 = 250$, $(W/L)_3 = 40$, and $(W/L)_4 = 80$.



Small-Signal Model:



KCL1:

$$(V_i - V_{o1})g_{m1} - g_{m2}V_{o1} = \frac{V_{o1}}{r_{o2}}$$

$$g_{m1}V_i - g_{m1}V_{o1} - g_{m2}V_{o1} = \frac{V_{o1}}{r_{o2}}$$

$$\frac{V_{o1}}{r_{o2}} + g_{m1}V_{o1} + g_{m2}V_{o1} = g_{m1}V_i$$

$$V_{o1}\left(\frac{1}{r_{o2}} + g_{m1} + g_{m2}\right) = g_{m1}V_i$$

$$\frac{V_{o1}}{V_i} = \frac{g_{m1}}{\left(\frac{1}{r_{o2}} + g_{m1} + g_{m2}\right)} = g_{m1}\cdot\left[r_{o2} \| \frac{1}{g_{m1}} \| \frac{1}{g_{m2}}\right]$$

$$= \frac{5m}{\frac{1}{20k} + 5m + 5m}$$

$$\frac{V_{out1}}{V_{in}} = 0.498\ V/V$$

KCL2:

$$-g_{m3}V_{o2} = \frac{V_{o2}}{r_{o4}} + (V_i - V_{o1})g_{m1}$$

$$-g_{m3}V_{o2} = \frac{V_{o2}}{r_{o4}} + g_{m1}V_i - g_{m1}V_{o1}$$

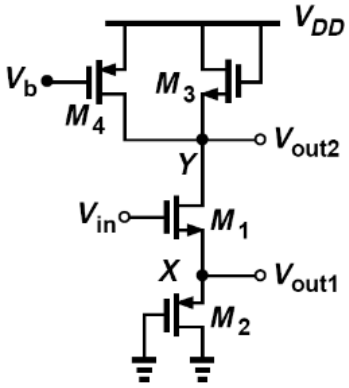
$$\frac{V_{o2}}{r_{o4}} + g_{m3}V_{o2} = g_{m1}V_i - g_{m1}\cdot\frac{g_{m1}}{\left(\frac{1}{r_{o2}} + g_{m1} + g_{m2}\right)}$$

$$V_{o2}\left(\frac{1}{r_{o4}} + g_{m3}\right) = g_{m1}V_i - g_{m1}\cdot\frac{g_{m1}}{\left(\frac{1}{r_{o2}} + g_{m1} + g_{m2}\right)}$$

$$V_{o2} = \frac{g_{m1}V_i - g_{m1}\cdot\frac{g_{m1}}{\left(\frac{1}{r_{o2}} + g_{m1} + g_{m2}\right)}}{\left(\frac{1}{r_{o4}} + g_{m3}\right)}$$

$$\frac{V_{out2}}{V_{in}} = -1.241\ V/V$$

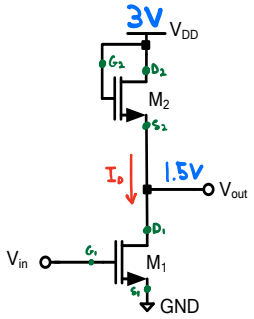
For your convenience the circuit and its parameters are duplicated below:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0.05\ V^{-1}$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5$V, $\mu_n C_{ox}=0.1$ mA/V^2, $\mu_p C_{ox}=0.05$ mA/V^2, and $\gamma_{(NMOS)}=\gamma_{(NMOS)}=0$.
$(W/L)_1 = 125$, $(W/L)_2 = 250$, $(W/L)_3 = 40$, and $(W/L)_4 = 80$.



2) Design a common-source amplifier with a diode-connected load based on the schematic shown below with the following design specifications:

- Transistor M1 is in saturation
- The minimum possible output voltage to keep M1 in saturation is 0.2V
- Total power consumption of the amplifier is 3mW
- Both transistors have L=0.5µm
- DC level of the output is 1.5 V

The technology parameters are:
λ(NMOS) = 0, γ = 0, V_{DD}=3V, V_{TH}(NMOS) = 0.5V, $\mu_n C_{ox}$=1 mA/V^2



Find the following values:
a) Width of the transistors, i.e., W_1 and W_2 **[5 marks]**,
b) DC level of the input **[5 marks]**,
d) Small-signal gain **[5 marks]**.
e) Maximum symmetric output signal swing while both transistors stay in saturation **[5 marks]**.

M_1: $V_{GD1} \leq V_{th} \rightarrow V_i - V_o \leq 0.5V$ to satisfy Saturation Requirement

$V_i = 0.5V + 0.2V \rightarrow V_i = 0.7V$

Power Consumption:

$P = I_D V_{DD} \rightarrow I_D = \frac{3mW}{3V} = 1mA$

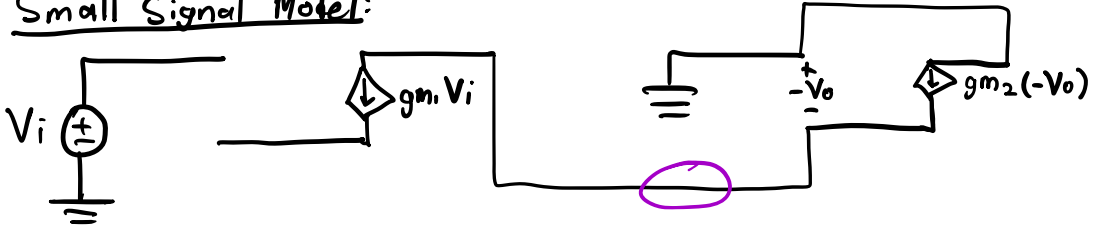
M_2:

$1mA = \frac{1}{2} \cdot 1\times10^{-3} \cdot \left(\frac{W}{L}\right)_2 \cdot (3-1.5-0.5)^2 \rightarrow \left(\frac{W_2}{0.5u}\right) = 2 \rightarrow W_2 = 1um$

M_1:

$1mA = \frac{1}{2} \cdot 1\times10^{-3} \cdot \left(\frac{W}{L}\right)_1 \cdot (0.7-0.5)^2 \rightarrow \left(\frac{W_1}{0.5u}\right) = 50 \rightarrow W_1 = 25um$

Small Signal Model:

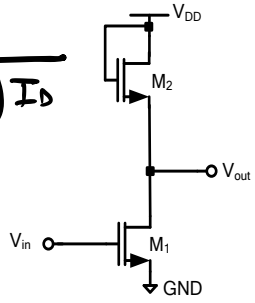


For your convenience the circuit and its parameters are duplicated below:
The technology parameters are:
$\lambda(NMOS) = 0$, $\gamma = 0$, $V_{DD}=3V$, $V_{TH}(NMOS) = 0.5V$, $\mu_n C_{ox}=1\ mA/V^2$

KCL: $-g_{m_2} V_o = g_{m_1} V_i$

$$\frac{V_o}{V_i} = \frac{-g_{m_1}}{g_{m_2}} \qquad g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

$$A_V = \frac{-\sqrt{2 \cdot 1\times10^{-3} \cdot 50 \cdot 1\times10^{-3}}}{\sqrt{2 \cdot 1\times10^{-3} \cdot 2 \cdot 1\times10^{-3}}}$$



$A_V = -5\ V/V$

e) $V_{out_{Min}} = 0.2V$, $V_{out_{DC}} = 1.5V$

Saturation Requirements:

$V_{GS_2} > V_{th} \longrightarrow V_{DD} - V_{out} > 0.5 \longrightarrow V_{out} = V_{DD} - 0.5 = 3V - 0.5V = 2.5V$

$2.5V - 1.5V = 1V$ to max

$1.5 - 0.2V = 1.3V$ to min

↳ Therefore, the symmetric swing (Peak to Peak) = 2V

DC level of input = 0.7 V,

DC level of output = 1.5 V, W_1= 25 µm, W_2= 1 µm,

small-signal gain A_V= -5 V/V,

maximum output swing (for a symmetric swing)= 2 V, (Peak-to-Peak)

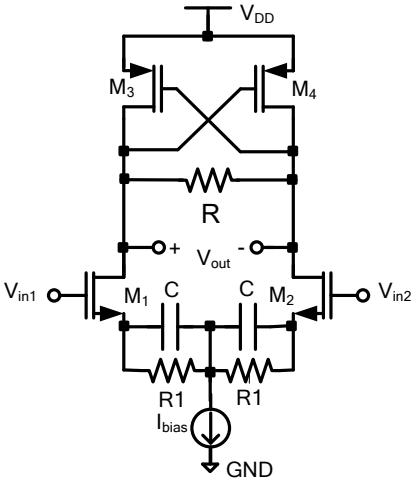
3. Assuming that the following circuit is symmetrical and $\gamma = \lambda = 0$:

i) Find the small-signal differential voltage gain ($\frac{V_{out}}{V_{in1} - V_{in2}}$) of the circuit at very low frequencies. **[7 marks]**

ii) What is the small-signal differential gain of the circuit at very high frequencies? **[7 marks]**

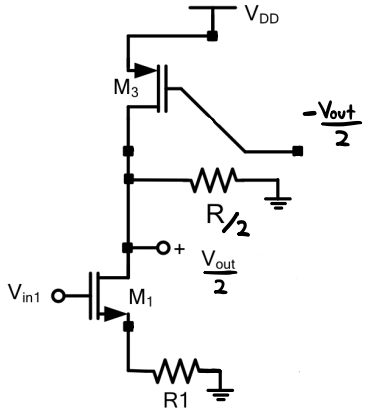
iii) For what value(s) of R the gain of parts (i) and (ii) will be maximized and what is the maximum gain? **[6 marks]**

Note: In this question neglect all other capacitances that are not shown in the circuit.



i) At very low frequencies, the capacitors are Open Circuits.

Half Circuit Model:

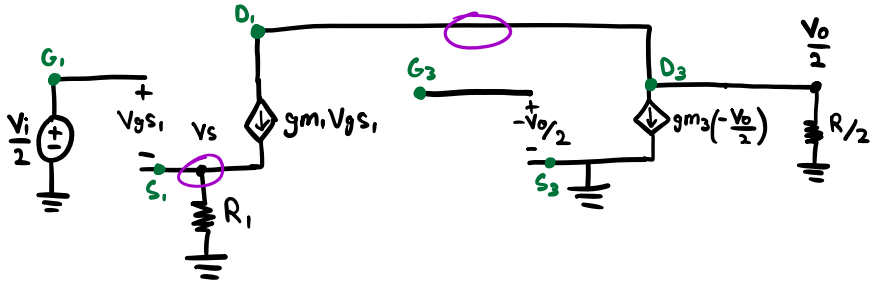


kVL_1: $\frac{V_i}{2} - V_{gs_1} = V_s$

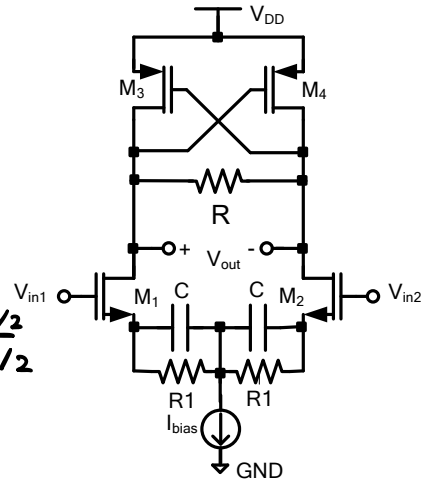
kCl_1: $g_{m_1} V_{gs_1} = \frac{V_s}{R_1}$

kCl_2: $0 = g_{m_1} V_{gs_1} + g_{m_3}\left(\frac{-V_o}{2}\right) + \frac{V_o/2}{R/2}$

Small-Signal Model:



For your convenience the circuit diagram is replicated here:



KVL$_1$: $\frac{V_i}{2} - V_{gs_1} = V_S$

KCL$_1$: $g_{m_1} V_{gs_1} = \frac{V_S}{R_1}$

KCL$_2$: $0 = g_{m_1} V_{gs_1} + g_{m_3}\left(\frac{-V_o}{2}\right) + \frac{V_o/2}{R/2}$

Solving for Gain:

$\frac{V_i}{2} = V_S + V_{gs_1}$

$\frac{V_i}{2} = g_{m_1} R_1 V_{gs_1} + V_{gs_1}$

$= \boxed{V_{gs_1}(1 + g_{m_1} R_1)}$

$\frac{V_o}{2} g_{m_3} - \frac{V_o}{R} = g_{m_1} V_{gs_1}$

$\frac{V_o}{2} \cdot \frac{g_{m_3}}{2} - \frac{V_o}{2} \cdot \frac{1}{R} = \frac{g_{m_1} V_{gs_1}}{2}$

$\frac{V_o}{2}\left(\frac{g_{m_3}}{2} - \frac{1}{R}\right) = \frac{g_{m_1} V_{gs_1}}{2}$

$\frac{V_o}{2} = \frac{g_{m_1}}{2} \cdot V_{gs_1} \cdot \left(\frac{1}{\frac{g_{m_3}}{2} - \frac{1}{R}}\right)$

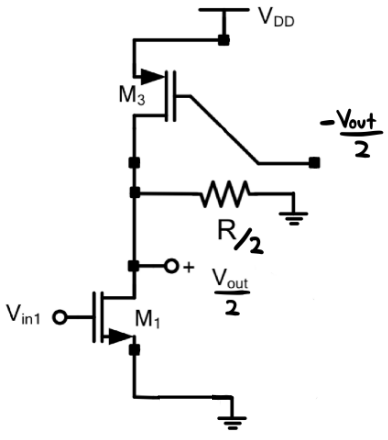
$= \boxed{\frac{g_{m_1} V_{gs_1}}{g_{m_3} - 2/R}}$

$\frac{V_o/2}{V_i/2} = \frac{\left(\frac{g_{m_1} V_{gs_1}}{g_{m_3} - 2/R}\right)}{V_{gs_1}(1 + g_{m_1} R_1)}$

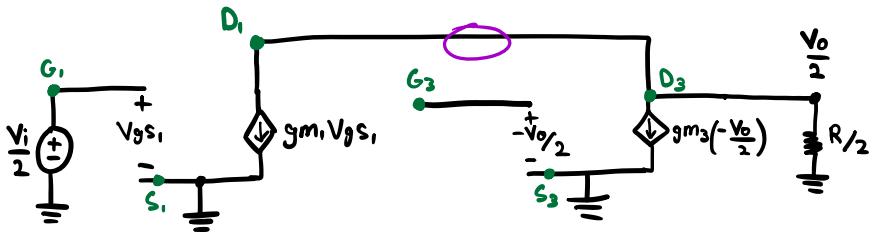
$A_V = \frac{g_{m_1}}{(g_{m_3} - 2/R)(1 + g_{m_1} R_1)} = \frac{-g_{m_1}}{(1 + g_{m_1} R_1)} \cdot \left[\frac{R}{2} \parallel \frac{-1}{g_{m_3}}\right]$

ii) At very high frequencies, the capacitors are shorted

Half Circuit Model:



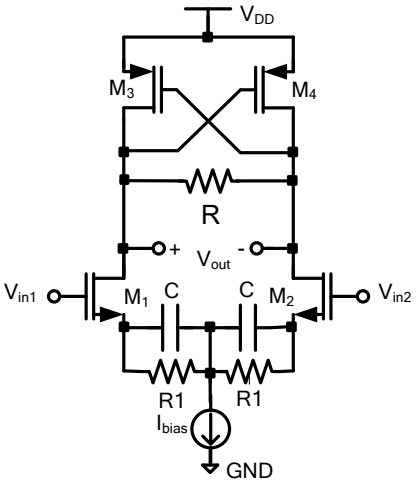
Small-Signal Model:



KVL$_1$: $\frac{V_i}{2} - V_{gs_1} = 0$

KCL$_1$: $0 = g_{m_1} V_{gs_1} + g_{m_3}\left(\frac{-V_o}{2}\right) + \frac{V_o/2}{R/2}$

For your convenience the circuit diagram is replicated here:



Solving for Gain:

$$\frac{v_i}{2} = V_{gs_1}$$

$$\frac{v_o}{2} g_{m_3} - \frac{v_o}{R} = g_{m_1} \frac{v_i}{2}$$

$$v_o g_{m_3} - 2\frac{v_o}{R} = g_{m_1} v_i$$

$$\rightarrow v_o(g_{m_3} - 2/R) = v_i g_{m_1}$$

$$\frac{v_o}{v_i} = \frac{g_{m_1}}{g_{m_3} - 2/R}$$

$$A_v = \frac{g_{m_1}}{g_{m_3} - 2/R} = -g_{m_1} \cdot \left[\frac{R}{2} \parallel \frac{-1}{g_{m_3}}\right]$$

iii) Part 1:

$$A_v = \frac{g_{m_1}}{(g_{m_3} - 2/R)(1 + g_{m_1} R_1)}$$

A_v max occurs when

$g_{m_3} - 2/R = 0$

$g_{m_3} = 2/R \rightarrow R = \frac{2}{g_{m_3}}$

The maximum gain is $3\ V/V$

Part 2:

$$A_v = \frac{g_{m_1}}{g_{m_3} - 2/R}$$

A_v max occurs when

$g_{m_3} - 2/R = 0$

$g_{m_3} = 2/R \rightarrow R = \frac{2}{g_{m_3}}$

The maximum gain is $3\ V/V$

4. In the follwing circuit assume that:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 50\mu A$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

Furthermore, assume that:

$$\left(\frac{W}{L}\right)_0 = \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 10$$

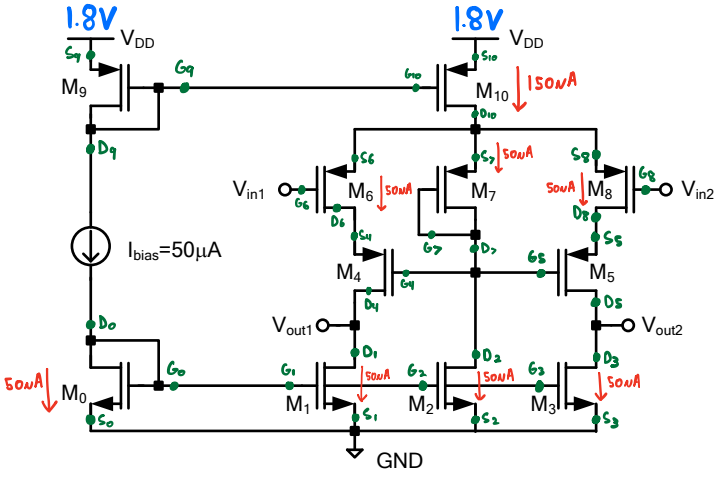
$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_9 = 20$$

$$\left(\frac{W}{L}\right)_7 = 5, \text{ and } \left(\frac{W}{L}\right)_{10} = 60$$

Given that the dc level of the inputs (i.e., input common mode) is 1.2 V:

i) Find the maximum and minimum voltage of V_{out1} and V_{out2} for which all devices stay in saturation. **[10 marks]**
ii) What is the differential output signal swing? **[2 marks]**
iii) Assuming that the circuit is driven by a differential input signal, find the magnitude of the differential gain of the circuit, when a resistor of value 20 kΩ is connected between V_{out1} and V_{out2}. **[8 marks]**

Note: Please note that the gates of M_0, M_1, M_2, and M_3 are connected to each other and none of these gates is connect to the bulk (body) of the transistors.



Currents:

M_0, M_1, M_2, M_3 (Same Aspect Ratio) → 50nA

$\left(\frac{W}{L}\right)_9 \cdot \frac{1}{3} = \left(\frac{W}{L}\right)_{10}$ → $I_{10} = 3I_9 =$ 150nA

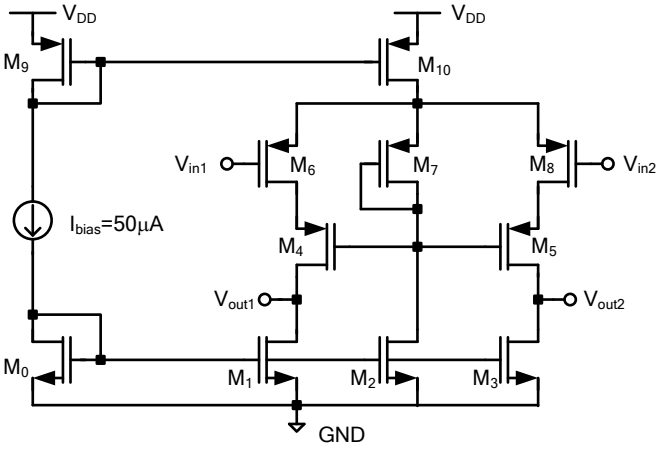
For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 50\mu A$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

NMOS: $V_D > V_G - V_{th}$

$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$

PMOS: $V_D < V_G - V_{th}$

$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)(V_{SG} - V_{th})^2$



M_1: Drain is connected to V_{out1}. Must satisfy Saturation Requirement

$50nA = \frac{1}{2} \cdot 1x10^{-3} \cdot 10(V_{eff1})^2 \rightarrow V_{eff1} = 0.1V \rightarrow V_{out_{Min}} = 0.1V$

M_7:

$50nA = \frac{1}{2} \cdot 0.5x10^{-3} \cdot 5 \cdot (V_{SG7} - 0.4)^2 \rightarrow V_{SG7} = 0.6V$

M_6:

$50nA = \frac{1}{2} \cdot 0.5x10^{-3} \cdot 20(V_{SG6} - 0.4)^2 \rightarrow V_{SG6} = 0.5V$

$0.5V = V_{SG6} - 1.2V \rightarrow V_{SG6} = 1.7V \rightarrow V_{S7} = V_{S8} = 1.7V$

$0.6V = 1.7V - V_{G7} \rightarrow V_{G7} = 1.1V \rightarrow V_{D7}, V_{G4}, V_{GS} = 1.1V$

M_4: Drain is connected to V_{out1}. Must satisfy Saturation Requirement

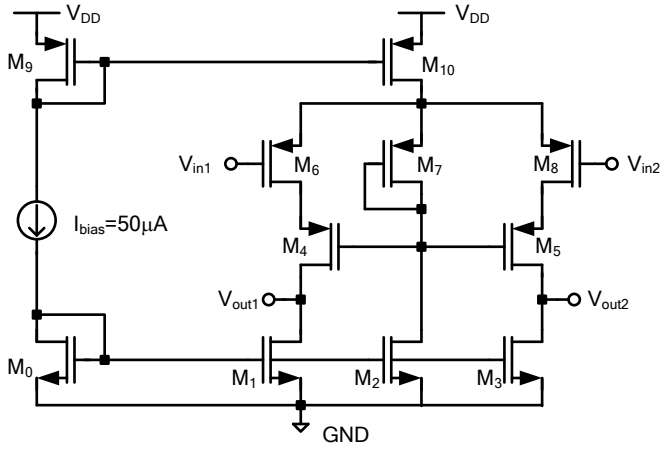
$V_{DG4} < |V_{th}|$

$V_{D4} - 1.1V < 0.4V$

$V_{D4} < 1.5V \rightarrow V_{out_{MAX}} = 1.5V$

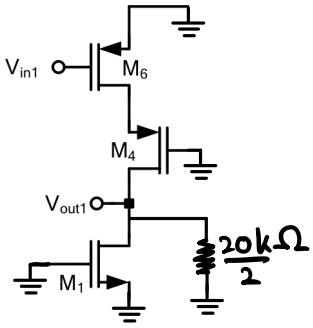
(ii) Differential output Swing $= 2(1.5 - 0.1) = 2.8V$

For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 50\mu A$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

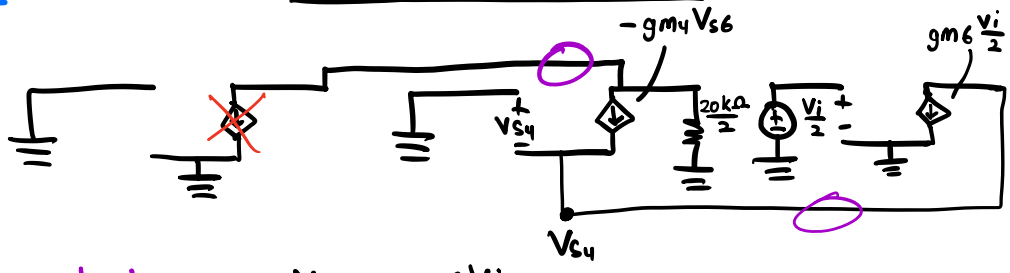


iii)

Half Circuit Model:



Small Signal Model:



KCL1: $-g_{m4}V_{s4} = g_{m6}\frac{V_i}{2}$

KCL2: $0 = -g_{m4}V_{s4} + \frac{V_o/2}{20k/2}$

$\frac{V_o}{20k} = g_{m4}V_{s4}$

$\frac{V_o}{20k} = -g_{m6}\frac{V_i}{2}$

$\frac{V_o}{V_i} = -g_{m6}\cdot\frac{20k\Omega}{2}$

$g_{m6} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_6 I_D}$

$= \sqrt{2\cdot 0.5\times10^{-3}\cdot 20\cdot 50\times10^{-6}}$

$= 1mA$

$\therefore |A_v| = 1\times10^{-3}\cdot\frac{20k\Omega}{2} = 10V/V$

$V_{out1,max}$= 1.5 V, $V_{out1,min}$= 0.1 V , $V_{out2,max}$= 1.5 V, $V_{out2,min}$= 0.1 V

Differential signal swing = 2.8 V, Differential gain= 10 V/V

5. In the following circuit assume:

$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$V, $\mu_n C_{ox}$=1 mA/V^2, $(W/L)_1$=$(W/L)_2$=324, $(W/L)_3$=$(W/L)_4$=100, R=0.5kΩ, R_D=0.5kΩ, C=200pF, C_L=2pF, and V_{bias}=0.7 V.

Ignoring all other parasitic device capacitances, and only taking into account the capacitors shown in the schematic diagram of the circuit, find the transfer function of the small-signal differential gain of the circuit, that is, $H(s) = \frac{V_{out+}(s) - V_{out-}(s)}{V_{in+}(s) - V_{in-}(s)}$ (where s is complex frequency in the Laplace domain). **[15 marks]**

Plot the bode plot of the magnitude of the frequency response, that is, bode plot of $|H(j\omega)|$ as a function of ω (for the frequency axis, use the angular frequency in radian per second instead of f in Hz, and provide the numerical value of the key angular frequencies, i.e., angular frequency of pole(s) and zero(s)). **[5 marks]**

Hint: For finding the transfer function, you may want to use the half-circuit concept and analyze the associated small-signal model in the Laplace domain, that is, use impedance of the components in your analysis.

Saturation Requirement:

NMOS: $V_D > V_G - V_{th}$

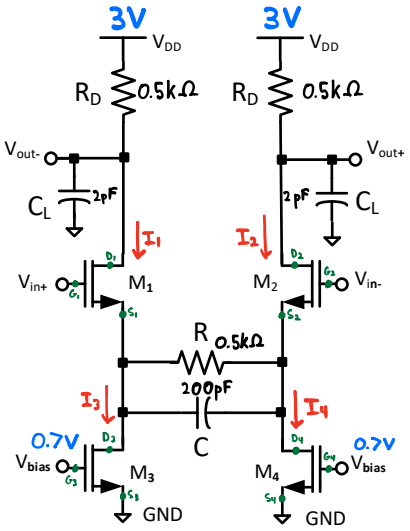
$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{th})^2$

$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$

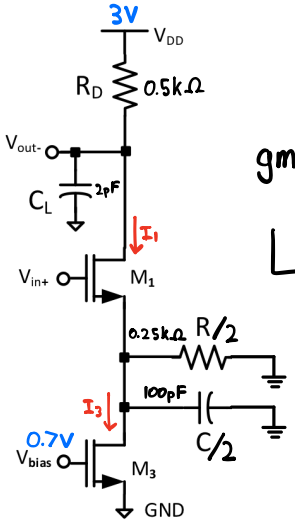
M_3:

$I_{D_3} = \frac{1}{2} \cdot 1\times10^{-3} \cdot 100 \cdot (0.7 - 0.5)^2$

$= 2mA \longrightarrow I_1 = 2mA$



Half-Circuit Model:

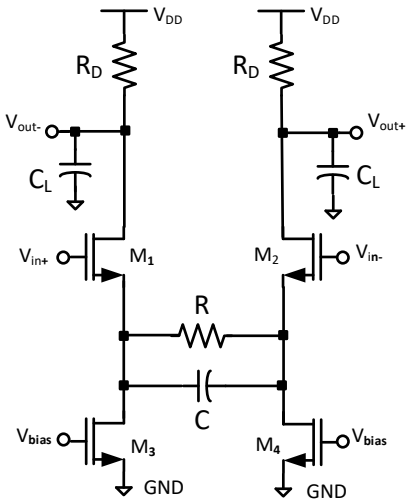


$g_{m_1} = \sqrt{2 \cdot 1\times10^{-3} \cdot 100 \cdot 2\times10^{-3}}$

$= 20mA/V$

$\longrightarrow g_{m_3} = 20mA/V$

For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$V, $\mu_n C_{ox}$=1 mA/V^2, $(W/L)_1$=$(W/L)_2$=324, $(W/L)_3$=$(W/L)_4$=100, R=0.5kΩ, R_D=0.5kΩ, C=200pF, C_L=2pF, and V_{bias}=0.7 V.

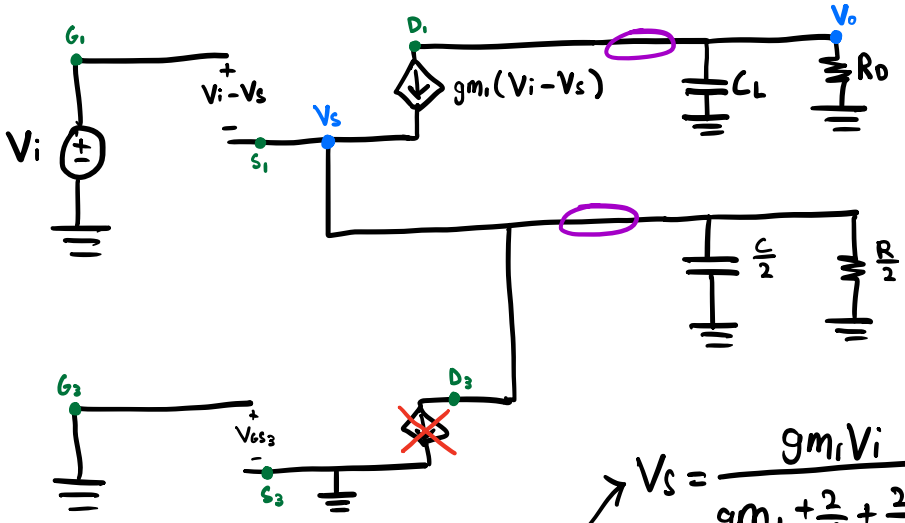


$V_{GD} < V_{th}$

$0.7 - V_S < 0.5$

$V_S = 1.2V$

Small-Signal Model:



$$V_S = \frac{g_{m1} V_i}{g_{m1} + \frac{2}{sC} + \frac{2}{R}}$$

KCL1:

$$g_{m1}(V_i - V_S) = \frac{V_S}{C/2} + \frac{V_S}{R/2}$$

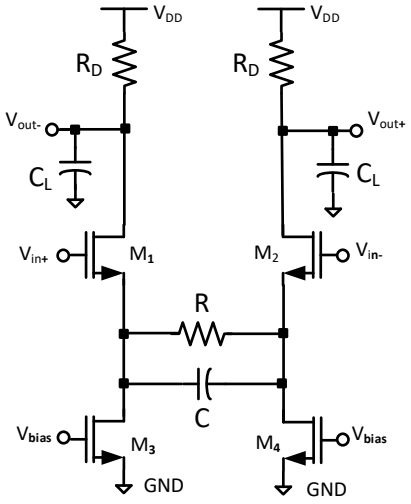
KCL2:

$$0 = g_{m1}(V_i - V_S) + \frac{V_o}{C_L} + \frac{V_o}{R_D}$$

$$V_S = \frac{g_{m1} C_L R_D V_i s + C_L V_o s + R_D V_o}{g_{m1} C_L R_D s}$$

$$\therefore \frac{g_{m1} V_i}{g_{m1} + \frac{2}{C} + \frac{2}{R}} = \frac{g_{m1} C_L R_D V_i s + C_L V_o s + R_D V_o}{g_{m1} C_L R_D s}$$

For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$V, $\mu_n C_{ox}$=1 mA/V^2, $(W/L)_1=(W/L)_2=324$, $(W/L)_3=(W/L)_4=100$, R=0.5kΩ, R_D=0.5kΩ, C=200pF, C_L=2pF, and V_{bias}=0.7 V.



$$\frac{g_{m_1} V_i}{g_{m_1} + \frac{2}{C} + \frac{2}{R}} = \frac{g_{m_1} C_L R_D V_i \cdot s + C_L V_o \cdot s + R_D V_o}{g_{m_1} C_L R_D \cdot s}$$

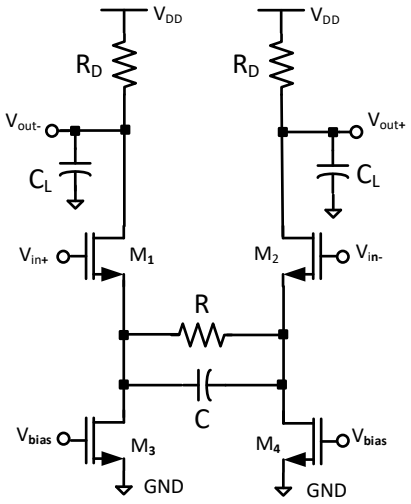
Solving for $\frac{V_o}{V_i}$ yields

$$H(s) = \frac{-4\times10^{-21} s^2 - 1\times10^{-8} s}{1.4\times10^{-21} s^2 + 3.51\times10^{-7} s + 250\times10^{3}}$$

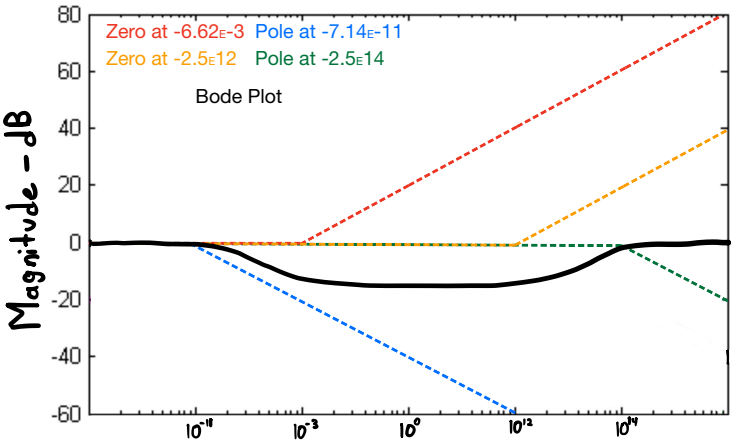
Zeros $\longrightarrow$ $s = -2.5\times10^{12},\ -6.62\times10^{-3}$

Poles $\longrightarrow$ $s = -2.5\times10^{14},\ -7.14\times10^{-11}$

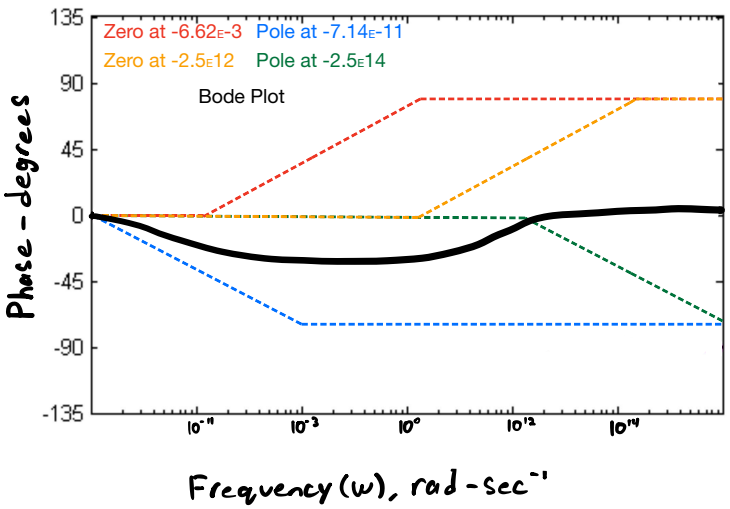
For your convenience the circuit diagram and parameters are replicated here:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$V, $\mu_n C_{ox}$=1 mA/V^2, $(W/L)_1=(W/L)_2$=324, $(W/L)_3=(W/L)_4$=100, R=0.5kΩ, R_D=0.5kΩ, C=200pF, C_L=2pF, and V_{bias}=0.7 V.



Magnitude Plot

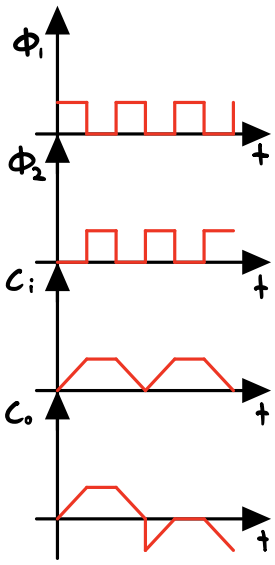


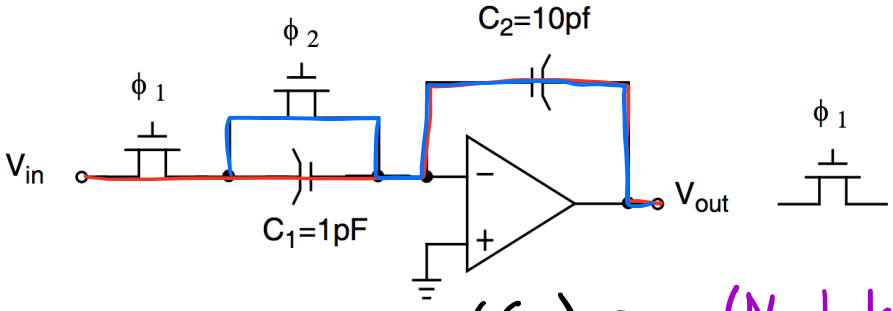
Phase Plot



Bonus Question: 6. Ignoring parasitic capacitances of the components, and assuming that the opamp is ideal and the switches are ideal and φ_1 and φ_2 are non-overlapping clocks, find the discrete-time transfer function of the following switched-capacitor circuit. **[20 marks]**

Hint 1: Note that when φ_1 is on (its associated switch is shorted) φ_2 is off (its associated switch is open) and vice versa. That is the two switches are not on at the same time. You may want to look at the relationship between the charge stored on the capacitors and use the similar analysis as that of slides 10 and 20 of Slide Set 7.
Hint 2: When the switch associated with φ_2 is on, capacitor C_1 is discharged that is charges on its left plate through the switch will combine and cancel the charges on its right plate!





$$H(z) = \frac{V_o(z)}{V_i(z)} \longrightarrow \left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$ (No delay)

$$C_2 V_{co}(nT - T/2) = C_2 V_{co}(nT - T)$$

$$C_2 V_{co}(nT) = C_2 V_{co}(nT - T/2) - C_1 V_{ci}(nT)$$

$$H(z) = \frac{\left(\frac{C_1 + C_2}{C_2}\right)z - \frac{C_2}{C_1}}{\left(1 + \frac{C_1}{C_2}\right) - z}$$

Where:
C_1=1pF
C_2=10pf